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OFGS File No. : P/2054-107
Inventor : Junji TAJIME et al
Title : MOVING PICTURE DECODING APPARATUS AND MOVING
PICTURE DECODING METHOD
Assignee : NEC Corporation

Enclosed herewith please find the following documents in the above-identified application for United States Letters Patent:

22 Pages of Specification including Abstract and Claims
18 Numbered Claims Calculated as 18 Claims for Fee Purposes
4 Sheets of Drawing Containing Figures 1 to 5.
X Declaration and Power of Attorney
X Priority is Claimed under 35 U.S.C. §119:
Convention Date June 19, 1998 for Japan Appln. S.N. 10-173179
X Certified Priority Application
X PTO-1449 with 3 references
X Assignment
X Return-Addressed Post Card

OFGS Check No. 85547, which includes the fee of \$800.00, calculated as follows:

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MOVING PICTURE DECODING APPARATUS AND MOVING PICTURE
DECODING METHOD

BACKGROUND OF THE INVENTION

5 The present invention relates to a moving picture
decoding apparatus, and especially, to a moving picture
decoding apparatus capable of reducing a capacity of a
frame memory when coded moving pictures are decoded.

10 Conventionally, this kind of a moving picture decoding
apparatus is used as a method for reducing a frame memory
capacity. As the conventional moving picture decoding
apparatus, in JP-A-261635/1997 for example, as an
arrangement for reducing a frame memory capacity necessary
for storage of reference images and re-ordering decoded
15 images, an arrangement is disclosed, which comprises a
data compression circuit for compressing a decoded image
and a data expansion circuit for expanding a compressed
data. Also, in JP-A-247673/1997, an arrangement is
proposed, in which a moving pictures data of which data
20 content has been reduced by data content reducing means
for reducing a data content of a decoded moving pictures
data is stored in a frame memory, and a data content of a
data read from the frame memory is restored by data
content restoring means.

25 Also, in JP-A-4550/1998 for example, an apparatus is

proposed, in which memory reduction is facilitated using Adaptive Differential Pulse Code Modulation (ADPCM). In the apparatus described in the publication, compression is conducted by estimating a change of each block of $n \times m$ pixels compressed using orthogonal translation, encoding a first pixel of each block with p bits in accordance with the ADPCM, encoding an estimated value of the change with $n \times h$ bits, and further, encoding a difference value between other each pixel following the first pixel and an average value of all pixels in the blocks with $p-k$ bits.

However, in the conventional moving picture decoding apparatus proposed in the above-described JP-A-4550/1998 and so forth, of which objective is to reduce capacity of the frame memory, there is a task that efficient access to the memory cannot be realized.

The reason thereof is that an access width of the memory is not at all taken into account in a memory compression and expansion section of the above-described moving picture decoding apparatus.

SUMMARY OF THE INVENTION

The objective of the present invention is to solve the above-mentioned.

Also, the objective thereof is to provide a moving picture decoding apparatus for reducing capacity of a

frame memory necessary when an image is decoded by means of compression operation and accomplishing compression and expansion processing of a memory content with a high speed, and further, for decoding an image with high quality.

5 For solving the above-described objective, the moving picture decoding apparatus of the present invention, to which a compressed stream generated using an inter-frame prediction system is input, comprises compression means for compressing a decoded image when the signal is stored
10 in a memory, expansion means for expanding a compressed image stored in the above-described memory, quantization means for controlling quantization on compression in the above-described compression means, and access width control means for controlling the above-described
15 quantization control means so that an information content for a single or a plurality of memory compression processing units or for every control unit of memory compression processing is in conformity with the bit number of an access unit of the above-described memory.

20 In the moving picture decoding apparatus of the present invention, said access width control means comprises means for controlling said quantization control means so that the coded bit number for a single or a plurality of compression processing units or for every control unit of
25 compression processing is in conformity with the bit

number of an access unit of said storage means in case that the coded bit number exceeds the bit number of an access unit of said storage means or is lacking.

5 Furthermore, in the moving picture decoding apparatus of the present invention, said compression means and expansion means conduct compression and expansion, respectively, in accordance with a pixel difference prediction encoding system.

10 Furthermore, the moving picture decoding apparatus of the present invention further comprising a plurality of quantizers and a plurality of quantization characteristic tables.

15 Furthermore, the moving picture decoding apparatus of the present invention further comprising a plurality of quantizers and a quantization characteristic table being shared by said plurality of quantizers.

20 Furthermore, in the moving picture decoding apparatus of the present invention, said compression means and expansion means conduct compression and expansion, respectively, in accordance with an orthogonal translation encoding system.

25 Furthermore, in the moving picture decoding apparatus of the present invention, said access width control means conducts control using information included in the compressed stream.

Furthermore, in the moving picture decoding apparatus of the present invention, said storage means is a frame memory.

5 **BRIEF DESCRIPTION OF THE DRAWINGS**

This and other objects, features and advantages of the present invention will become more apparent upon a reading of the following detailed description and drawings, in which:

10 Fig. 1 is a block diagram showing an arrangement of a moving picture decoding apparatus of the first embodiment of the present invention;

15 Fig. 2 is a view for explaining the principle of the present invention and a view for showing an access bit width and a width of a quantized data;

 Fig. 3 is a view for explaining the principle of the present invention and a view for showing an access bit width and a width of a quantized data;

20 Fig. 4 is a view for showing an arrangement of a memory compression and expansion section in the first embodiment of the present invention and

 Fig. 5 is a block diagram showing an arrangement of the second embodiment of the present invention.

DESCRIPTION OF THE EMBODIMENTS

25 A form of working of the present invention will be

explained. In a preferable form of working of a moving picture decoding apparatus in the present invention, compression is applied to a decoded image in a memory compressor (105 of Fig. 1), and it is stored in a frame memory (106 of Fig. 1). Based on an occupied content of the frame memory (106 of Fig. 1), in case that the coded data bit number for a single or a plurality of memory compression processing units or for every control unit of memory compression processing exceeds the bit number of a memory access unit or is lacking, a memory access width control section (110 of Fig. 1) applies control to a quantizer control section (109 of Fig. 1) so that the coded data bit number is conformed to be equal to or less than the bit number of the memory access unit.

First, the principle of the present invention will be explained. A decoded image is compressed using various compression methods. However, the coded data bit number per compression processing unit, which is allocated by compression operation, is allocated based on a compression ratio, and the bit number of a memory access unit is not taken into account.

It is assuming that the bit number of the memory access unit is $M1$ bits, the coded data bit numbers of a compression processing unit, which is allocated based on a compression ratio, are $N1, N2, N3, \dots, Nn$, respectively,

and $M1 < N1 + N2 + \dots + Nn$. In this case, a coded data of n blocks cannot be extracted through one access.

Accordingly, by decreasing the bit number allocated by $N1 + N2 + \dots + Nn$ by $N1 + N2 + \dots + Nn - M1$, an allocated bit
5 can be made equal to or less than $M1$, and therefore, the coded data can be taken out through one access.

An example of $n = 3$ as the n blocks is shown in Fig. 2. By subtracting more than or equal to $M2$ ($M2 = (N1 + N2 + N3) - M1$) bits from $N1 + N2 + N3$ bits, an allocated bit
10 can be made equal to or less than $M1$.

On the other hand, as shown in Fig. 3, in case that the allocated bit is less than the bit number $M1$ of a memory access unit, and a frame memory has capacity, allocation of the bit number of the coded data can be also increased.

In the present invention, on the basis of such a
15 principal, the memory access width control section (110 of Fig. 1) applies control of an access width of the frame memory to the quantization control section.

In a from of working of the present invention, the
20 memory compressor and memory expander may have an arrangement in which compression and expansion are conducted, respectively, in accordance with DPCM.

In a from of working of the present invention, based on access width information from the access width control
25 section, in case that a generated information content for

5 a single or a plurality of memory compression processing
units or for every control unit of memory compression
processing exceeds the bit number of a memory access unit,
quantization control is conducted by preparing a plurality
of quantizers having different quantization
characteristics, and a quantization table, and by
selecting a quantizer that is adapted to an access width.
In this case, an arrangement may be adopted, in which one
quantization table is shared by the plurality of
10 quantizers having different quantization characteristics.
In other words, by variably changing a reference interval
of one quantization table in accordance with an obtained
quantization characteristic (resolution and so forth), it
is possible to obtain the different quantization
15 characteristics while one quantization table is shared.

Also, in a form of working of the present invention, the
memory compressor and the memory expander may conduct
compression and expansion, respectively, in accordance
with an orthogonal translation encoding system.

20 Moreover, in a form of working of the present invention,
the access width control section may apply access width
control to the quantization control section using
information included in the compressed stream. Below, a
detailed explanation will be made in accordance with an
25 embodiment.

The first embodiment of the present invention will be explained in detail by referring to drawings. Fig. 1 is a view showing an arrangement of one embodiment of the present invention.

Referring to Fig. 1, this embodiment is constructed by comprising a variable length decoder 101, an inverse quantizer 102, an inverse discrete cosine transducer (Inverse DCT) 103, an adder 104, a motion compensation section 108, and a memory compression and expansion section 11. The memory compression and expansion section 11 is constructed by comprising a memory compressor 105, a frame memory 106, a memory expander 107, a quantizer control section 109, and a memory width control section 110.

A compressed moving pictures stream encoded by a system such as an ISOIS13818-2 (MPEG-2VIDEO) is supplied as an input to the variable length decoder 101.

The variable length decoder 101 performs variable length decoding, and supplies a result thereof to the inverse quantizer 102.

The inverse quantizer 102 performs inverse quantization, and supplies a result thereof to the inverse discrete cosine transducer 103.

The inverse discrete cosine transducer 103 transduces a conversion coefficient into an image, and supplies a

result thereof to the adder 104.

The adder 104 performs addition of the image supplied from the inverse discrete cosine transducer 103 and a predicted image supplies from the motion compensation section 108, and supplies a result thereof to the memory compression and expansion section 11.

The memory compression and expansion section 11 applies compression and expansion operation to a decoded image, and supplies it to the motion compensation section 108.

The motion compensation section 108 performs motion compensation based on a motion vector supplied from the variable length decoder 101 and the image supplied from the memory compression and expansion section 11, and supplies the predicted image to the adder 104.

The memory compressor 105 of the memory compression and expansion section 11 applies compression to the image supplied from the adder 104, and stores it in the frame memory 106.

The memory expander 107 extracts the compressed image from the frame memory 106 and expands it, and supplies it to the motion compensation section 108.

The quantization control section 109 applies control for quantization of the image to the memory compressor 105 and the memory expander 107.

The access width control section 110 applies control to

the quantization control section 109 using information of the frame memory 106 so that an information content for a single or a plurality of memory compression processing units or for every control unit of memory compression processing is conformed to be equal to or less than the bit number of a memory access unit.

As the compression encoding in the memory compressor and the memory expander, pixel difference encoding, adaptive pixel difference encoding, DCT translation, Hadamard translation, and Wavelet translation and so forth, for example, are used.

Fig. 4 is a view showing one example of an arrangement of the memory compression and expansion section 11 in one embodiment of the present invention in case that the memory compressor 105 and the memory expander 107 are constructed of the pixel difference encoding. The memory compressor 105 and the memory expander 107 in Fig. 1 correspond to a memory compressor 21 and a memory expander 23 in Fig. 4.

Referring to Fig. 4, the memory compressor 21 is constructed by comprising a subtracter 201, a quantizer 202, a fixed-length decoder 203, an inverse quantizer 204, an adder 205, and a predictor 206. The memory expander 23 is constructed by comprising a fixed-length decoder 207, an inverse quantizer 208, an adder 209, and a predictor

210.

An image to be compressed is supplied to the subtracter 201 as an input, and the subtracter 201 performs subtraction of this input signal and a predicted value supplied from the predictor 206, and supplies a prediction error to the quantizer 202.

The quantizer 202 performs quantization of the prediction error in accordance with the quantization control section 24, and supplies it to the fixed-length decoder 203 and the inverse quantizer 204.

The fixed-length decoder 203 encodes the quantized value and stores it in the frame memory 22. In the inverse quantizer 204, the adder 205 and the predictor 206, inverse quantization and local decoding are performed, and an output from the predictor 206 is supplied to the subtracter 201.

The memory access width control section 25 takes account of a compression ratio based on an occupied ratio of the frame memory 22, and applies bit allocation control to the quantization control section 24, which is in conformity with the bit number of a memory access unit.

The quantization control section 24 performs quantization control in which memory access width information is added, and applies control to the quantizer 202 so that an information content generated for a single

or a plurality of memory compression processing units or for every control unit of memory compression processing is to be equal to or less than the bit number of a memory access unit.

5 In this embodiment, if the compression processing unit is assumed to be constant, a block of a single pixel or a plurality of $m \times n$ pixels becomes to be a compression processing unit.

10 The memory expander 23 receives a compressed image from the frame memory 22, and performs expansion of the compressed image by applying expansion and inverse quantization thereto, and outputs the image.

15 Next, an example will be explained, in which one memory access width control is realized. One quantizer having a fixed compression ratio is used for quantization of a prediction error. In such a case, in case that an information content generated for a single or a plurality of memory compression processing units or for every control unit of memory compression processing exceeds the bit number of a memory access unit, a plurality of
20 quantizers are prepared, and control is conducted so that the information content is in conformity with an access width. In this example, since an occupied content of the frame memory can be fixed, information from the frame
25 memory is not required. In addition, an arrangement can be

adopted, in which a plurality of quantizers having quantization characteristics different from each other share one quantization characteristic table.

On the other hand, in a case of orthogonal translation and so forth, it is difficult to fix an information content generated for a single or a plurality of memory compression processing units or for every control unit of memory compression processing. In such a case, use of an occupied content of the frame memory is convenient.

Next, the second embodiment of the present invention will be explained. In the above-described first embodiment, the access width control section 110 conducts control of the quantizer control section 109 using the access memory width and the occupied content of the frame memory.

Fig. 5 is a view showing an arrangement of the second embodiment of the present invention. Referring to Fig. 5, in the second embodiment of the present invention, the access width control section 110 receives information from the inverse quantizer 102, and applies control to the quantization control section 109, in which information included in a compressed stream is added, in other words, in which information during quantization is added.

Accordingly, by taking account of the information of the compressed stream and a relation between positions on an image, and so forth, allocation of the information content

can be realized, which makes image quality be improved.

As explained above, in accordance with the present invention, advantages are effected as described below.

The first advantage of the present invention is that
5 compression and expansion processing for the contents of the memory can be conducted with a high speed.

The reason thereof is that, in the present invention, since quantization control which is to be equal to or less than the number of bits of a memory access unit is
10 conducted, the number of a memory access to the compressed image necessary for the expansion is reduced.

The second advantage of the present invention is that, by conducting allocation control of an information content using the information included in the compressed stream,
15 an error of an pixel can be suppressed and image quality can be improved.

The reason thereof is that, in the present invention, by taking account of the information of the compressed stream and a relation between positions on an image, and so forth,
20 allocation of the information content can be realized, which makes image quality be improved.

What is claimed is:

1 A moving picture decoding apparatus to which a compressed stream generated using an inter-frame prediction system is input, said apparatus comprises:

5 compression means for compressing a decoded image when the signal is stored in storage means;

 expansion means for expanding a compressed image stored in said storage means;

10 quantization control means for controlling quantization on compression in said compression means; and

 access width control means for controlling said quantization control means so that bit allocation control is conducted so as to be in conformity with the bit number of an access unit of said storage means.

15 2 A moving picture decoding apparatus according to claim 1, wherein said access width control means comprises means for controlling said quantization control means so that the coded bit number for one or a plurality of compression processing units or for every control unit of compression processing is in conformity with the bit number of an access unit of said storage means in case that the coded bit number exceeds the bit number of an access unit of said storage means or is lacking.

20 3 A moving picture decoding apparatus according to claim 1, wherein said compression means and expansion means

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conduct compression and expansion, respectively, in accordance with a pixel difference prediction encoding system.

4 A moving picture decoding apparatus according to claim 1, further comprising a plurality of quantizers and a plurality of quantization characteristic tables.

5 A moving picture decoding apparatus according to claim 1, further comprising a plurality of quantizers and a quantization characteristic table being shared by said plurality of quantizers.

6 A moving picture decoding apparatus according to claim 1, wherein said compression means and expansion means conduct compression and expansion, respectively, in accordance with an orthogonal translation encoding system.

7 A moving picture decoding apparatus according to claim 1, wherein said access width control means conducts control using information included in the compressed stream.

8 A moving picture decoding apparatus according to claim 1, wherein said storage means is a frame memory.

9 A moving picture decoding apparatus to which a compressed stream generated using an inter-frame prediction system is input, said apparatus comprises:

compression means for compressing a decoded image;

storage means for storing a compressed image in said

compression means;

expansion means for expanding the compressed image
stored in said storage means;

quantization control means for controlling quantization
5 on compression in said compression means; and

said access width control means for applying bit
allocation control to said quantization control means so
as to be in conformity with the bit number of an access
unit of said storage means, and

10 said quantization control means controls quantization in
said compression means based on access width information
from said access width control means so that generated
information content for one or a plurality of compression
processing units or for every control unit of compression
15 processing is equal to or less than the bit number of an
access unit of said storage means in case that the
generated information content exceeds the bit number of an
access unit of said storage means or is lacking.

10 A moving picture decoding apparatus according to claim
20 9, wherein said access width control means applies bit
allocation control to said quantization control means so
as to be in conformity with the bit number of an access
unit of said storage means, based on an occupied content
of said storage means.

25 11 A moving picture decoding apparatus according to claim

9, wherein said access width control means conducts control using information included in the compressed stream.

12 A moving picture decoding apparatus according to claim 5 9, wherein said access width control means applies control to said quantization control means so that, compared with the bit number of an access unit of said storage means, in case that the allocation bit number of a coded data of a compression processing unit exceeds the bit number of an access unit of said storage means or less than the bit number of an access unit of said storage means, the allocation bit number is equal to or less than the bit number of an access unit of said storage means by subtracting a predetermined number of bits from the allocation bit number of a coded data of said compression processing unit or by increasing the allocation bit number by the predetermined number of bits, whereby the coded data can be taken out by means of one access to said storage means.

13 A moving picture decoding apparatus according to claim 20 9, wherein said compression means controls quantization characteristic of quantizer for quantizing said decoded image, based on control of said quantization control means.

14 A moving picture decoding apparatus according to claim 25 9, further comprises a plurality of quantizers having

quantization characteristics different from each other,
and a quantization characteristic table is shared by said
plurality of quantizers.

15 A moving picture decoding apparatus according to claim
5 9, wherein said compression means comprises a subtracter,
a quantizer, an encoder, an inverse quantizer, an adder,
and predictor,

a prediction error that is obtained in said subtracter
by a subtraction between said decoded image and a
10 predicted value from said predictor is supplied to said
quantizer,

under control of said quantization control means, said
quantizer quantizes said prediction error and supplies it
to said encoder and said inverse quantizer,

15 said encoder encodes an output from said quantizer and
outputs it to said storage means, and

inverse quantization and local decoding are conducted in
said inverse quantizer, said adder, and said predictor.

16 A moving picture decoding apparatus according to
20 claim 9, wherein said storage means is a frame memory.

17 A moving picture decoding method comprising the steps
of:

detecting the coded bit number for one or a
plurality of compression processing units or for every
25 control unit of compression processing and

controlling said coded bit number so that said coded
bit number is in conformity with the bit number of an
access unit of a storage means when said detected coded
bit number exceeds the bit number of an access unit of
said storage means or is lacking.

5

18 A moving picture decoding method according to claim 17,
wherein said step of controlling comprise a step of
controlling using information included in the compressed
stream.

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ABSTRACT

A memory compression and expansion section (11 of Fig. 1) applies compression to a decoded image, and it is stored in a frame memory. Based on an occupied content of the frame memory (Fig. 1 106), in case that the coded bit number for a single or a plurality of memory compression processing units or for every control unit of memory compression processing exceeds the bit number of a memory access unit or is lacking, a memory access width control section (110 of Fig. 1) applies control to a quantizer control section (109 of Fig. 1) so that the coded bit number is conformed to be equal to or less than the bit number of the memory access unit.

FIG.1

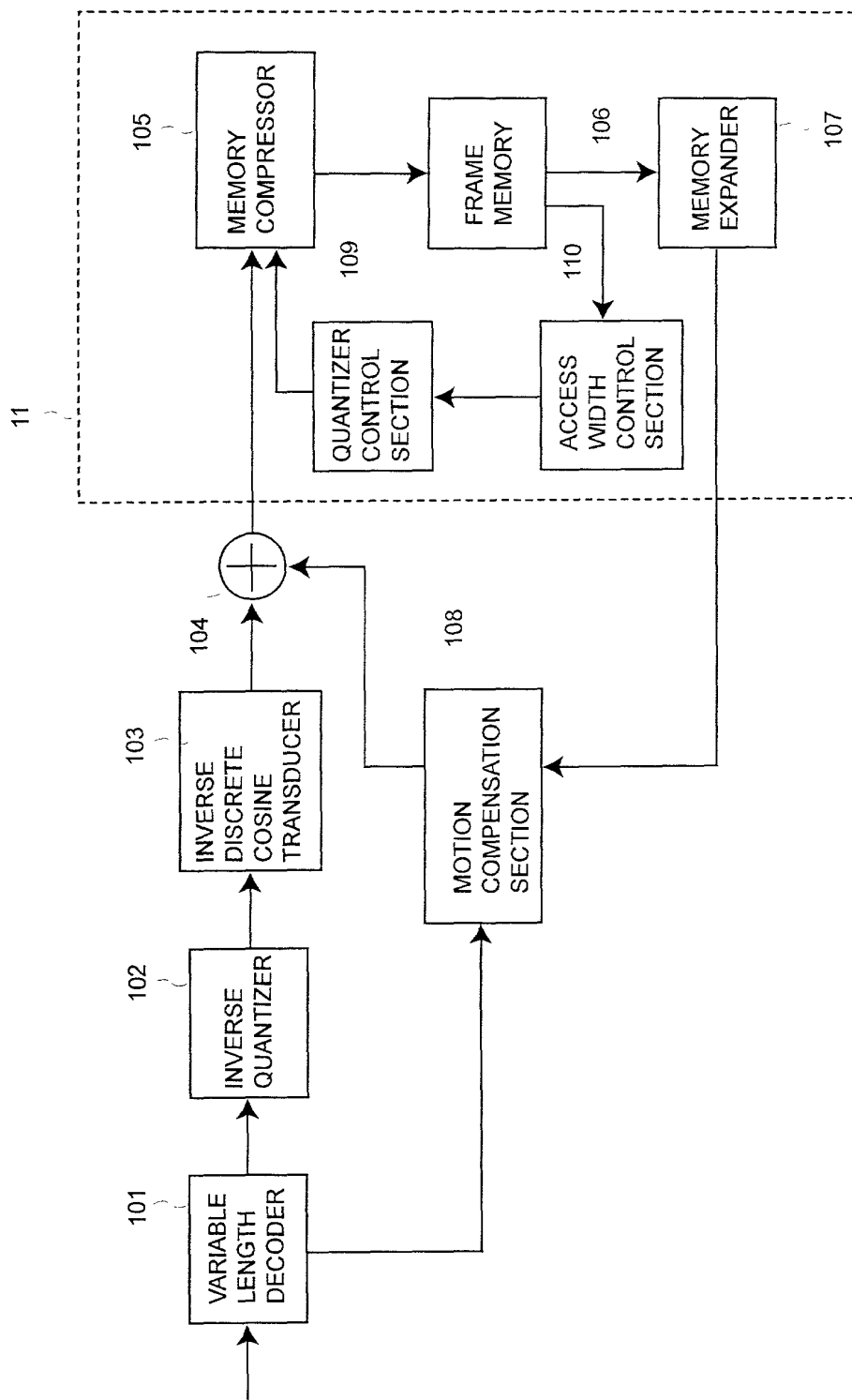


FIG.2

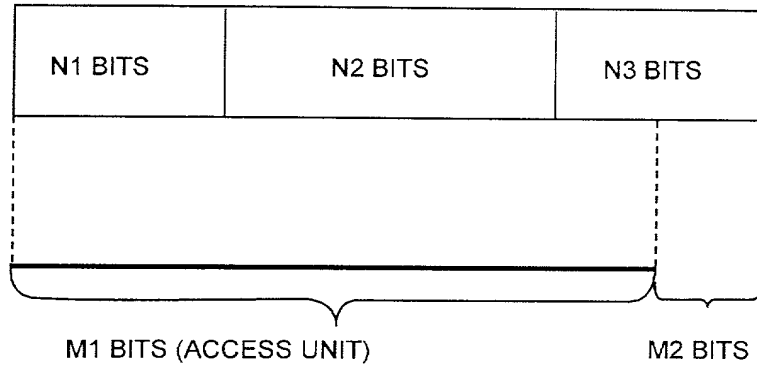


FIG.3

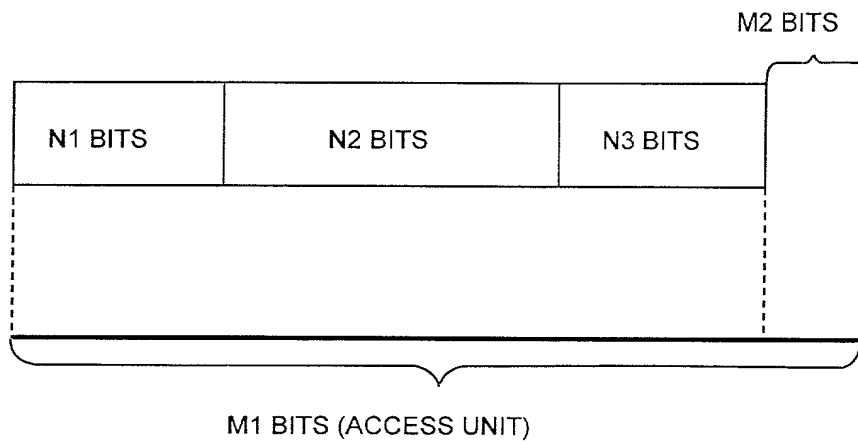


FIG.4

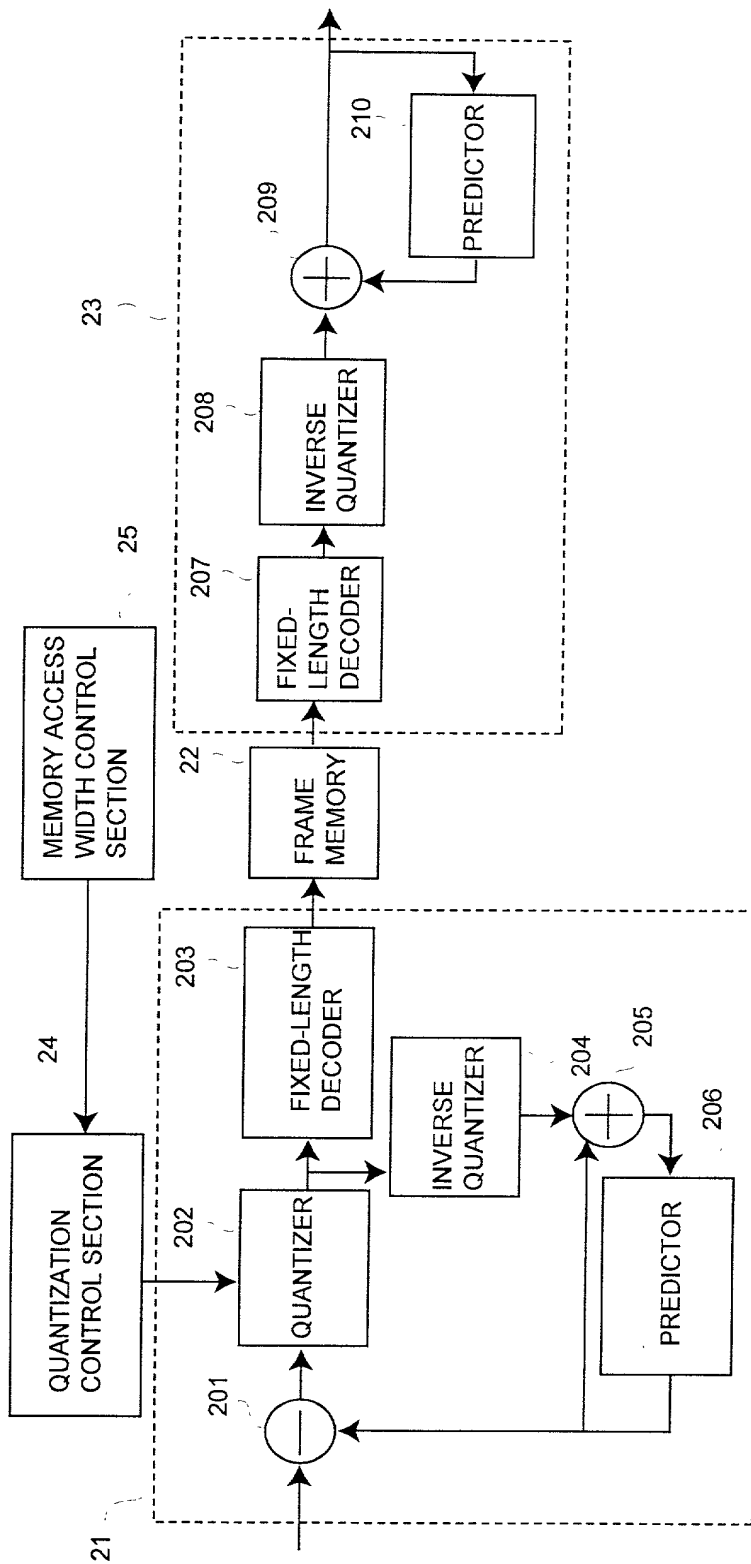
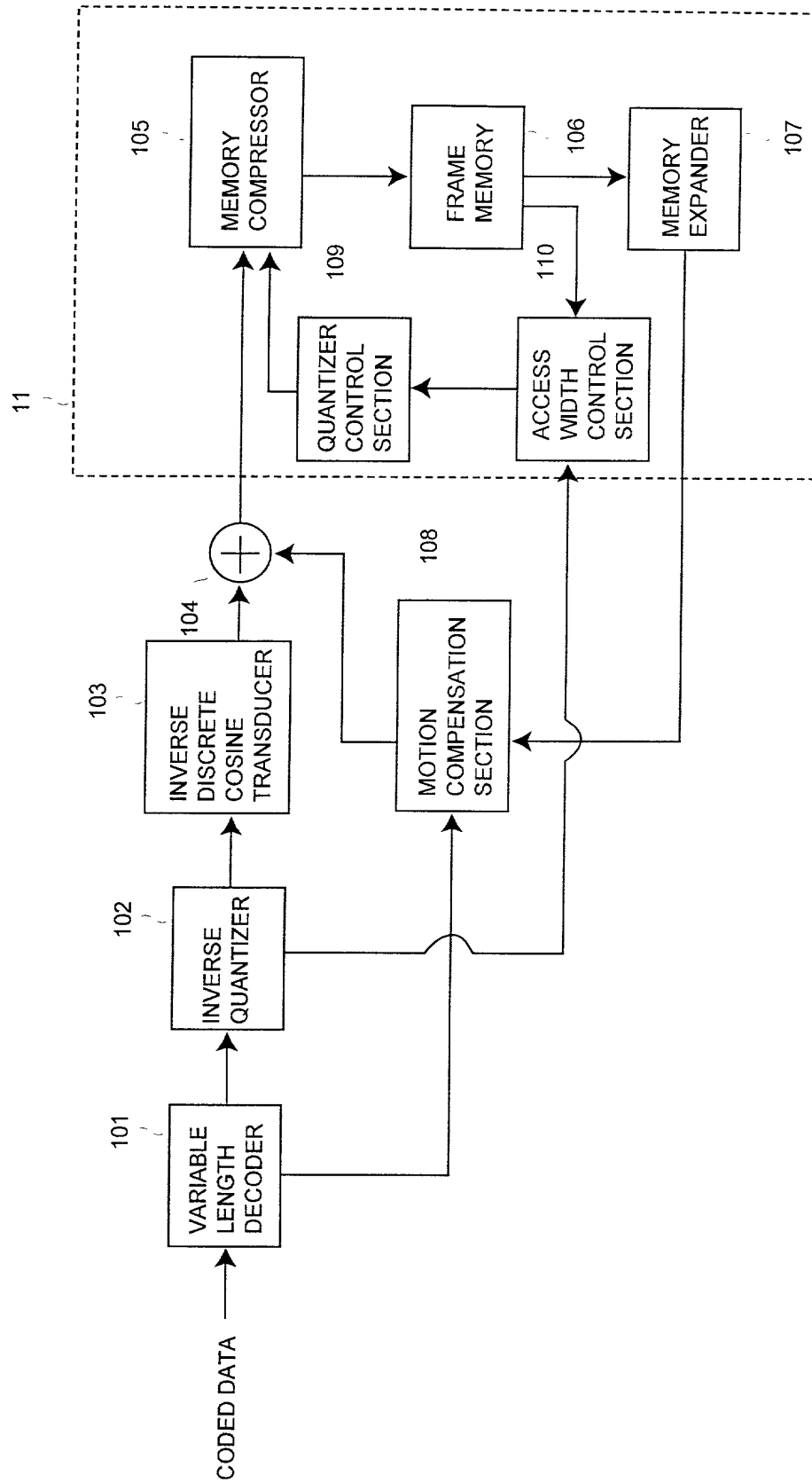


FIG.5



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UNITED STATES OF AMERICA COMBINED DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION		OFGS FILE NO. P/2054-107																																																								
<p>As a below named inventor, I hereby declare that: my residence, post office address and citizenship are as stated below next to my name; that I verily believe that I am the original, first and sole inventor (if only one name is listed below) or a joint inventor (if plural inventors are named) of the subject matter which is claimed and for which a patent is sought on the invention entitled:</p> <p style="text-align: center;">MOVING PICTURE DECODING APPARATUS AND MOVING PICTURE DECODING METHOD</p> <p>the specification of which is attached hereto, unless the following box is checked:</p> <p><input type="checkbox"/> was filed on _____ as United States patent Application Number or PCT International patent application number _____ and was amended on _____ (if any).</p> <p>I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.</p> <p>I acknowledge the duty to disclose all information known to be material to patentability in accordance with Title 37, Code of Federal Regulations, §1.56.</p> <p>I hereby claim priority benefits under Title 35, United States Code §119 of any foreign application(s) for patent or inventor's certificate or United States provisional application(s) listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:</p> <p>Prior Foreign or Provisional Application(s)</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 25%;">COUNTRY</th> <th style="width: 25%;">APPLICATION NUMBER</th> <th style="width: 25%;">DATE OF FILING (day, month, year)</th> <th style="width: 25%;">PRIORITY CLAIMED UNDER 35 U.S.C. 119</th> </tr> </thead> <tbody> <tr> <td>Japan</td> <td>10-173179</td> <td>19, 06, 1998</td> <td>YES <input checked="" type="checkbox"/> NO <input type="checkbox"/></td> </tr> <tr> <td> </td> <td> </td> <td> </td> <td>YES <input type="checkbox"/> NO <input type="checkbox"/></td> </tr> <tr> <td> </td> <td> </td> <td> </td> <td>YES <input type="checkbox"/> NO <input type="checkbox"/></td> </tr> </tbody> </table> <p>I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, §1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 30%;">UNITED STATES APPLICATION NUMBER</th> <th style="width: 30%;">DATE OF FILING (day, month, year)</th> <th style="width: 40%;">STATUS (patented, pending, abandoned)</th> </tr> </thead> <tbody> <tr><td> </td><td> </td><td> </td></tr> <tr><td> </td><td> </td><td> </td></tr> <tr><td> </td><td> </td><td> </td></tr> </tbody> </table> <p>I hereby appoint OSTROLENK, FABER, GERB & SOFFEN, LLP, and the members of the firm, Marvin C. Soffen - Reg. No. 17,542; Samuel H. Weiner - Reg. No. 18,510; Jerome M. Berliner - Reg. No. 18,653; Robert C. Faber - Reg. No. 24,322; Edward A. Meilman - Reg. No. 24,735; Stanley H. Lieberstein - Reg. No. 22,400; Steven I. Weisburd - Reg. No. 27,409; Max Moskowitz - Reg. No. 30,576; Stephen A. Soffen - Reg. No. 31,063; James A. Finder - Reg. No. 30,173; William O. Gray, III - Reg. No. 30,944 and Louis C. Dujmich - Reg. No. 30,625, as attorneys with full power of substitution and revocation to prosecute this application, to transact all business in the Patent & Trademark Office connected therewith and to receive all correspondence.</p> <p>SEND CORRESPONDENCE TO: OSTROLENK, FABER, GERB & SOFFEN, LLP 1180 AVENUE OF THE AMERICAS NEW YORK, NEW YORK 10036-8403</p> <p>DIRECT TELEPHONE CALLS TO: (212) 382-0700</p> <p>I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 35%;">FULL NAME OF SOLE OR FIRST INVENTOR Junji TAJIME</td> <td style="width: 25%;">INVENTOR'S SIGNATURE <i>Junji Tajime</i></td> <td style="width: 10%;">DATE June 14, 1999</td> </tr> <tr> <td colspan="2">RESIDENCE (City and either State or Foreign Country) Tokyo, Japan</td> <td>COUNTRY OF CITIZENSHIP Japan</td> </tr> <tr> <td colspan="3">POST OFFICE ADDRESS c/o NEC Corporation, 7-1, Shiba 5-chome, Minato-ku, Tokyo, Japan</td> </tr> </table> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 35%;">FULL NAME OF SECOND JOINT INVENTOR (IF ANY) Tetsuro TAKIZAWA</td> <td style="width: 25%;">INVENTOR'S SIGNATURE <i>Tetsuro Takizawa</i></td> <td style="width: 10%;">DATE June 14, 1999</td> </tr> <tr> <td colspan="2">RESIDENCE (City and either State or Foreign Country) Tokyo, Japan</td> <td>COUNTRY OF CITIZENSHIP Japan</td> </tr> <tr> <td colspan="3">POST OFFICE ADDRESS c/o NEC Corporetion, 7-1, Shiba 5-chome, Minato-ku, Tokyo, Japan</td> </tr> </table> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 35%;">FULL NAME OF THIRD JOINT INVENTOR (IF ANY)</td> <td style="width: 25%;">INVENTOR'S SIGNATURE</td> <td style="width: 10%;">DATE</td> </tr> <tr> <td colspan="2">RESIDENCE (City and either State or Foreign Country)</td> <td>COUNTRY OF CITIZENSHIP</td> </tr> <tr> <td colspan="3">POST OFFICE ADDRESS</td> </tr> </table>				COUNTRY	APPLICATION NUMBER	DATE OF FILING (day, month, year)	PRIORITY CLAIMED UNDER 35 U.S.C. 119	Japan	10-173179	19, 06, 1998	YES <input checked="" type="checkbox"/> NO <input type="checkbox"/>				YES <input type="checkbox"/> NO <input type="checkbox"/>				YES <input type="checkbox"/> NO <input type="checkbox"/>	UNITED STATES APPLICATION NUMBER	DATE OF FILING (day, month, year)	STATUS (patented, pending, abandoned)										FULL NAME OF SOLE OR FIRST INVENTOR Junji TAJIME	INVENTOR'S SIGNATURE <i>Junji Tajime</i>	DATE June 14, 1999	RESIDENCE (City and either State or Foreign Country) Tokyo, Japan		COUNTRY OF CITIZENSHIP Japan	POST OFFICE ADDRESS c/o NEC Corporation, 7-1, Shiba 5-chome, Minato-ku, Tokyo, Japan			FULL NAME OF SECOND JOINT INVENTOR (IF ANY) Tetsuro TAKIZAWA	INVENTOR'S SIGNATURE <i>Tetsuro Takizawa</i>	DATE June 14, 1999	RESIDENCE (City and either State or Foreign Country) Tokyo, Japan		COUNTRY OF CITIZENSHIP Japan	POST OFFICE ADDRESS c/o NEC Corporetion, 7-1, Shiba 5-chome, Minato-ku, Tokyo, Japan			FULL NAME OF THIRD JOINT INVENTOR (IF ANY)	INVENTOR'S SIGNATURE	DATE	RESIDENCE (City and either State or Foreign Country)		COUNTRY OF CITIZENSHIP	POST OFFICE ADDRESS		
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